(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 537 781 A1

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 92117751.5

(22) Date of filing: 16.10.92

(51) Int. Cl.5: H01L 31/068, H01L 31/0352

(30) Priority: 17.10.91 JP 269568/91

(43) Date of publication of application: 21.04.93 Bulletin 93/16

(84) Designated Contracting States: CH DE FR GB LI

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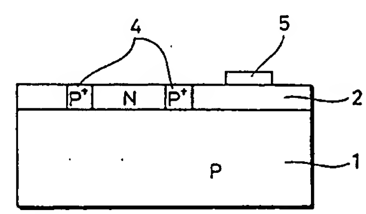
(54) Solar cell.

(57) A solar cell includes a first semiconductor region (1) of a P type, a second semiconductor region (2) of an N type made in contact with the first semiconductor region (1) so as to form a PN junction, and a third semiconductor region (4) of a P^+ type made in contact with both the first and second semiconductor regions (1, 2) and having a higher impurity concentration than that of the first semiconductor region (1).

FIG. 1A



EP 0 537 781 A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to solar batteries and, more particularly, to a solar cell which enables prevention of an accident caused by a reverse bias voltage generated, for example, when a solar cell module is shaded.

Description of the Background Art

Fig. 12 is a top plan view showing a typical example of a solar cell of background art; Fig. 13 is a cross-sectional view taken along the line B-B of Fig. 12; and Fig. 14 is a bottom view of the solar cell of Fig. 12. As can be seen in Figs. 12, 13 and 14, a light receiving surface of the solar cell is coated with a transparent anti-reflection film 8. Comb tooth-like or grid-like front electrodes 7 are provided beneath the anti-reflection film 8. One end of each of the front electrodes 7 is connected to an electrode connecting portion 5 which is a so-called bar electrode or contact electrode. Further, the solar cell includes a P type region 1 occupying a large part of a silicon substrate, an N type region 2 formed on an upper side surface of the P type region 1, and a P^+ region 3 for a BSF (back surface field) effect, formed on a lower side surface of the P type region 1. A back electrode 6 is provided to cover an approximately overall lower side surface of the P^+ region 3.

The solar cell of Fig. 13 can be manufactured, for example, by the following process.

First, a P type silicon substrate 1 shown in Fig. 15A is prepared.

With reference to Fig. 15B, a P^+ region 3 is formed by diffusion on an overall surface of the P type silicon substrate 1 of Fig. 15A.

Referring to Fig. 15C, the P^+ region 3 on an upper side surface of the silicon substrate 1 is then removed by etching.

After that, an N type region 2 is formed on an upper side surface of the P type silicon substrate 1 as shown in Fig. 15D.

With reference to Fig. 15E, a comb tooth-like front electrode 7 (not shown) and an electrode connecting portion 5 are formed on the N type region 2. At least the N type region 2 is coated with an anti-reflection film 8. A back electrode 6 is provided on a lower surface of the P^+ region 3. With a resultant structure cut along broken lines indicated on opposite sides of Fig. 15E, the solar cell shown in Fig. 13 is obtained.

It is rare that the solar cell shown in Fig. 12 is used alone. Normally, in order to obtain a desired output voltage and a desired output current, a solar cell module M in which a plurality of solar cells are connected in series and in parallel is formed, as shown in Fig. 16A.

Incidentally, when the solar cell module M is in practical use, a part of the module M is sometimes shaded In the case with a solar cell module M for use in space, it is possible that the shadow of a part of a main body of a satellite or the shadow of such a structure as antenna is casted on the solar cell module M during, for example, attitude control of satellites. Further, in the case with a solar cell module M for terrestrial use, it sometimes happens that the shadows of trees or buildings are casted on the solar cell module M and that droppings of birds cast a shadow on the solar cell module M.

Referring to Figs. 16A and 16B, the solar cell module M in which some of solar cells are shaded is illustrated. That is, a shadow is casted on a submodule 10 including a plurality of solar cells arranged in parallel. With reference to Fig. 16A, a voltage V_{11} generated from another submodule 11 which is unshaded is applied as a reverse bias voltage to the shaded submodule 10 in a shunt mode in which the opposite ends of the solar cell module M are almost short-circuited. A relation $V_{10} = -V_{11}$ is satisfied where a voltage of the submodule 10 is V_{10}. When the solar cell module M is connected with an external power supply V_B, a relation $V_{10} = V_B - V_{11}$ is satisfied as shown in Fig. 16B.

That is to say, when a positive voltage is applied to a front electrode of the shaded submodule 10 of the solar cell module M and a reverse bias voltage of the applied positive voltage exceeds a reverse withstanding voltage of the solar cell, the solar cells in the submodule 10 are led to incur short-circuit damages, thereby deteriorating output characteristics of the entire solar batter module M.

In order to prevent such an accident caused by the reverse bias voltage in the solar batter module M, a method is known in which a bypass diode is connected for each solar cell or each submodule including a certain number of solar cells. In addition, such a method is known that a so-called diode integrated solar cell is employed in which bypass diodes are integrated on solar cell cells themselves.

The method of connecting bypass diodes has such problems that a manufacturing cost of the solar cell module increases in proportion to the number of bypass diodes to be used and that a light receiving area on the solar cell decreases only by an area necessary for connection of the bypass diodes.

In addition, in the diode integrated solar cell, since both the diodes and solar cells must be integrated onto silicon substrate, its manufacturing method becomes complicated. That is, the manu-

facturing cost of the diode integrated solar cell becomes higher as compared to that of a normal solar cell.

SUMMARY OF THE INVENTION

In view of the foregoing background art, an object of the present invention is to provide a solar cell at a low cost in which a short-circuit damage caused by a reverse bias voltage can be prevented.

A solar cell in accordance with present invention includes a first semiconductor region of a P type, a second semiconductor region of an N type made in contact with the first semiconductor region to form a PN junction, and a third semiconductor region of a P type made in contact with both the first semiconductor region and the second semiconductor region and having an impurity concentration higher than that of the first semiconductor region.

When a reverse bias voltage is applied to the solar cell of the present invention, the PN junction between the first and second semiconductor regions and a P^+N junction between the second and third semiconductor regions are reverse-biased. At that time, a breakdown due to a Zener effect is more liable to occur in the P^+N junction between the second and third semiconductor regions as compared to the PN junction between the first and second semiconductor regions. That is, when a relatively small reverse bias voltage is applied to the solar cell, the P^+N junction between the second and third semiconductor regions causes a certain magnitude of backward current, and if the reverse bias voltage becomes higher, a Zener breakdown takes place. This can prevent a breakdown in the PN junction between the first and second semiconductor regions, which is necessary in the solar cell.

Fig. 11 shows an equivalent circuit of the solar cell of the present invention. That is, the solar cell in accordance with the present invention includes a solar cell having a PN junction, and a diode which has a P^+N junction and is connected in parallel with that PN solar cell. Consequently, if a reverse bias is applied to the solar cell of the present invention, then a current flows through the P^+N junction having a relatively large backward leakage, whereby the PN solar cell can be protected from a breakdown.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B and 1C are cross-sectional views of solar batteries of various types in accordance with the present invention.

Fig. 2 is a top view of a solar cell according to one embodiment of the present invention.

Fig. 3 is a cross-sectional view taken along the line A-A of Fig. 2.

Figs. 4A - 4F are cross-sectional views showing steps of manufacturing the solar cell of Fig. 3.

Fig. 5 is a top view of a solar cell according to another embodiment of the present invention.

Fig. 6 is a cross-sectional view taken along the line A_1 - A_1 of Fig. 5.

Figs. 7A - 7E are cross-sectional views showing steps of manufacturing the solar cell of Fig. 6.

Fig. 8 is a top view of a solar cell according to still another embodiment of the present invention.

Fig. 9 is a cross-sectional view taken along the line A_2 - A_2 of Fig. 8.

Figs. 10A - 10F are cross-sectional views showing steps of manufacturing the solar cell of Fig. 9.

Fig. 11 is a diagram of an equivalent circuit of a solar cell of the present invention.

Fig. 12 is a top view of a solar cell of background art.

Fig. 13 is a cross-sectional view taken along the line B - B of Fig. 12.

Fig. 14 is a bottom view of the solar cell of Fig. 12.

Figs. 15A - 15E are cross-sectional views showing steps of manufacturing the solar cell of Fig. 13.

Figs. 16A and 16B are top views showing a solar cell module.

In the above figures, identical reference characters denote their corresponding portions.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to Figs. 1A, 1B and 1C, solar batteries of various types according to various embodiments of the present invention are illustrated in schematic cross-sectional views. The structures of these types may be combined together.

In the solar cell of Fig. 1A, an N type semiconductor region 2 is formed on a top surface of a P type semiconductor region 1. A plurality of island-like P^+ regions 4 are formed in the N type region 2. These P^+ regions 4 are made not in contact with a front electrode (not shown).

In the solar cell of Fig. 1B, successive P^+ regions 4 or a plurality of divided P^+ regions 4 are formed along peripheries of an N type region 2 formed on a top surface of a P type region 1. Any

of the P^+ regions 4 is made not in contact with a front electrode (not shown).

In the solar cell of Fig. 1C, a plurality of well-like P^+ regions 4 are formed on a top surface of a P type region 1. These P type region 1 and P^+ regions 4 are covered with an N type region 2.

Fig. 2 is a top view of the solar cell which belongs to the type of Fig. 1A; and Fig. 3 is a cross-sectional view taken along the line A-A of Fig. 2. The solar cell shown in Figs. 2 and 3 includes an anti-reflection film 8, an N type region 2, a P type region 1, a P^+ region 3, a back electrode 6, comb tooth-like front electrodes 7 and an electrode connecting portion 5, similarly to the solar cell shown in Figs. 12 and 13.

The solar cell shown in Figs. 2 and 3, however, includes in addition to the above elements, a plurality of small island-like P^+ regions 4 locally formed in the N type region 2. Those island-like P^+ regions 4 are formed so as not to be in contact with any of the comb tooth-like electrodes 7.

Since the island-like P^+ regions 4 have a higher impurity concentration than that of the P type region 1, a P^+N junction formed between the island-like P^+ regions 4 and the N type region 2 has the property that a breakdown due to a Zener effect is liable to occur. The P^+ regions 4 may have an impurity concentration of not less than $1x10^{18}cm^{-3}$ in order to cause the Zener effect.

The solar cell of Fig. 3 can be manufactured by, e.g., the following process.

First, a P type silicon substrate 1 shown in Fig. 4A is prepared.

With reference to Fig. 4B, a P^+ region 3 is formed on an overall surface of the P type substrate 1 by diffusing P^+ impurities of a concentration of, e.g., approximately $1x10^{19}$ - $5x10^{22}cm^{-3}$ into the P type silicon substrate 1.

With reference to Fig. 4C, an overall lower surface and predetermined portions of an upper surface of the silicon substrate 1 are covered with an acid-resistant resin 9 such as a photoresist. Instead, an acid-resistant tape may be attached on the overall lower surface of the silicon substrate 1.

With reference to Fig. 4D, the silicon substrate 1 in the state of Fig. 4C is then etched by being dipped into an etching solution consisting such as of a mixed acid of a hydrofluoric acid and a nitric acid. After that, the acid-resistant resin 9 is removed.

Then, as shown in Fig. 4E, an N type region 2 is formed on the upper surface of the silicon substrate 1 by thermal diffusion. At this time, the surface of P^+ regions 4 is protected by a boron glass layer employed as a P type impurity source. However, a careful attention must be paid to setting of a diffusion depth so as to prevent N type impurities from entering too deeply into each P^+ region 4 of a high concentration from its opposite sides and thus damaging the P^+ region 4.

With reference to Fig. 4F, comb tooth-like front electrodes 7 (not shown) and an electrode connecting portion 5 are formed on the upper surface of the silicon substrate 1. Further, an anti-reflection film 8 and a back electrode 6 are formed, respectively, on the upper surface and the lower surface of the silicon substrate 1 by vacuum evaporation or the like. After that, cutting the resultant structure along broken lines on the opposite sides of Fig. 4F results in the solar cell shown in Fig. 3.

Since the manufacturing method illustrated in Figs. 4A - 4F is not so complicated as the conventional manufacturing method shown in Figs. 15A - 15E, the manufacturing cost of the solar cell of Fig. 3 does not increase much.

The size of each of the island-like P^+ regions 4 and the number of the P^+ regions 4 need to be adjusted depending on the size and the type of each solar cell and each module. In general, in a solar cell having an area of 2cm x 2cm, each P^+ region 4 may be in the form of a circle with a diameter of 0.01 - 1.0mm or of a quadrilateral with one side of 0.01 - 1.0mm. In addition, the P^+ regions 4 are preferably provided by a number within the range of 10 - 100. If a total area of the island-like P^+ regions 4 becomes too large, output characteristics of the solar cell deteriorate. It is thus desirable to design the solar cell so that the total area of the P^+ regions 4 is made as small as possible while satisfying conditions on which a Zener breakdown takes place in the P^+ regions 4 before the solar cell is damaged.

Fig. 5 is a top plan view of a solar cell which belongs to the type of Fig. 1B; and Fig. 6 is a cross-sectional view taken along the line A_1 - A_1 of Fig. 5. The solar cell shown in Figs. 5 and 6 is also similar to the one show in Figs. 12 and 13. However, the solar cell shown in Figs. 5 and 6 additionally includes a plurality of small P^+ regions 4 formed locally along peripheries of an upper surface of the solar cell. The solar cell of Fig. 6 can be manufactured by, e.g., the following process.

First, a P type silicon substrate 1 is prepared as shown in Fig. 7A.

With reference to Fig. 7B, a P^+ region 3 is formed on an overall surface of the P type substrate 1 by diffusing P type impurities of a concentration of, e.g., approximately $1x10^{19}$ to $5x10^{22}cm^{-3}$ into the P type silicon substrate 1.

Referring to Fig. 7C, a paste P including N type impurities of a high concentration is applied onto a predetermined region on the upper surface of the silicon substrate 1. A silicon oxide film or a nitride film doped with N type impurities of a high concentration may be deposited by a CVD (Chemical vapor Deposition) method in place of the

paste P.

With reference to Figs. 7C and 7D, the paste P is baked and an N type region 2 is formed.

As shown in Fig. 7E, comb tooth-like front electrodes 7 (not shown) and an electrode connecting portion 5 are then formed on the upper surface of the silicon substrate 1, and an anti-reflection film 8 is formed thereon by vacuum evaporation or the like. A back electrode 6 is formed on a lower surface of the silicon substrate 1 by vacuum evaporation or the like. Finally, cutting the resultant structure along broken lines on the opposite sides of Fig. 7E results in the solar cell shown in Fig. 6.

Since the manufacturing method illustrated in Figs. 7A - 7E is also not so complicated as the conventional manufacturing method shown in Figs. 15A - 15E, the manufacturing cost of the solar cell of Fig. 6 does not increase much.

Fig. 8 is a top view of a solar cell which belongs to the type of Fig. 1C; and Fig. 9 is a cross-sectional view taken along the line A_2 - A_2 of Fig. 8. The solar cell shown in Figs. 8 and 9 is similar to one shown in Figs. 2 and 3; however, island-like P^+ regions 4 shown in Figs. 8 and 9 are different in shape from those shown in Figs. 2 and 3. The solar cell of Fig. 9 can be manufactured by, e.g., the following process.

First, a P type silicon substrate 1 shown in Fig. 10A is prepared.

With reference to Fig. 10B, an oxide film 9 is formed on an overall surface of the silicon substrate 1 by thermal oxidation or the like.

Referring then to Fig. 10C, a plurality of openings 14 are formed in predetermined positions in the oxide film 9 on an upper surface of the silicon substrate 1.

As shown in Figs. 10C and 10D, boron is diffused to an extent of approximately $1x10^{20}cm^{-3}$ through the openings 14 in the oxide film, thereby forming a plurality of island-like P^+ regions 4. Here, the island-like P^+ regions 4 should be formed deeper than an N type region 2 which is to be formed at the next step. After that, the entire oxide film 9 is removed.

With reference to Fig. 10E, the N type region 2 is formed on the surface of the silicon substrate 1 by thermal diffusion or the like. At this step, the P^+ regions 4 are buried under the N type region 2. After that, at least the upper surface side of the silicon substrate is coated with an acid-resistant resin such as a photoresist, and thereafter, the N type region 2 on at least the lower surface of the silicon substrate 1 is etched away with a mixed solution of a hydrofluoric acid and a nitric acid.

With reference to Fig. 10F, comb tooth-like front electrodes 7 (not shown) and an electrode connecting portion 5 are formed on the upper surface of the silicon substrate 1, and an anti-reflection film 8 is formed thereon by vacuum evaporation or the like. A back electrode 6 is formed on the lower surface of the silicon substrate 1 by vacuum evaporation or the like. Finally, cutting the resultant structure along broken lines on the opposite sides of Fig. 10F results in the solar cell shown in Fig. 9.

Since the manufacturing method illustrated in Figs. 10A - 10F is also not so complicated as the conventional manufacturing method shown in Figs. 15A - 15E, the manufacturing cost of the solar cell of Fig. 9 does not increase much.

In the step of Fig. 10C, a photoresist may be employed in place of the oxide film 9 formed thermally and then the P^+ regions 4 may be formed by employing ion implantation in place of thermal diffusion.

In the solar cell of the type of Fig. 1C, it is not possible that P^+ regions 4 come into contact with front electrodes 7. Therefore, the P^+ regions 4 can be formed below the front electrodes 7 in the solar cell of the type of Fig. 1C.

While no description has been given with respect to solar batteries of a BSF type and a BSFR (BSF and back surface reflector) type in the foregoing embodiments, it will be understood that the present invention is applicable to any one of the BSF type and the BSFR type of solar batteries.

Further, while the description has been given on the case with use of the P type silicon substrate in the foregoing embodiments, it will be understood that an N type silicon substrate and substrates other than a silicon single crystal substrate, such as a GaAs substrate may also be employed in the present invention.

It will also be understood that the present invention is applicable to both of a solar cell for space use and a solar cell for terrestrial use.

As described above, according to the present invention, it is possible to provide a solar cell at a low cost in which a short-circuit damage due to a reverse bias voltage is less liable to occur. In particular, in the case with a space solar cell module which is difficult in maintenance, the present invention can exert a prominent effect on protection of the solar cell against a reverse bias voltage and enhance reliability of the entire solar cell module. Moreover, since the solar cell in accordance with present invention does not require any bypass diode, the cost of the solar cell is further reduced.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A solar cell, comprising:
   a first semiconductor region (1) of a P type;
   a second semiconductor region (2) of an N type made in contact with said first semiconductor region (1) so as to form a PN junction; and
   a third semiconductor region (4) of a P^{+} type made in contact with both of said first and second semiconductor regions (1, 2) and having an impurity concentration higher than an impurity concentration of said first semiconductor region (1).

2. The solar cell of claim 1, wherein said third semiconductor region (4) includes a plurality of island-like regions formed in said second semiconductor region (2).

3. The solar cell of claim 1, wherein said third semiconductor region (4) is formed along a periphery of said second semiconductor region (2).

4. The solar cell of claim 3, wherein said third semiconductor region (4) is divided into a plurality of regions.

5. The solar cell of claim 1, wherein said third semiconductor region (4) is formed as a plurality of well-like regions extending from an interface of said PN junction to said first semiconductor region (1).

6. The solar cell of claim 1, wherein said solar cell is of either type selected from the group consisting of a BSF type and a BSFR type.

7. The solar cell of claim 1, wherein said semiconductor is comprised of one selected from the group constituting of silicon and GaAs.

FIG. 1A

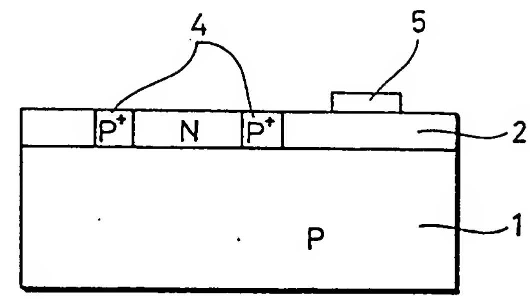


FIG. 1B

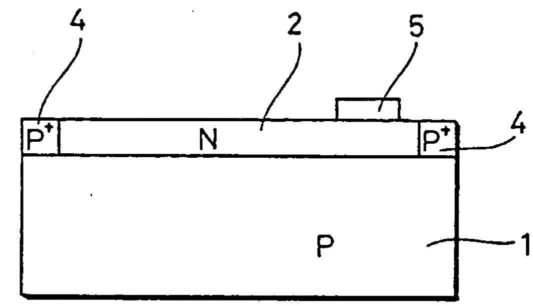


FIG. 1C

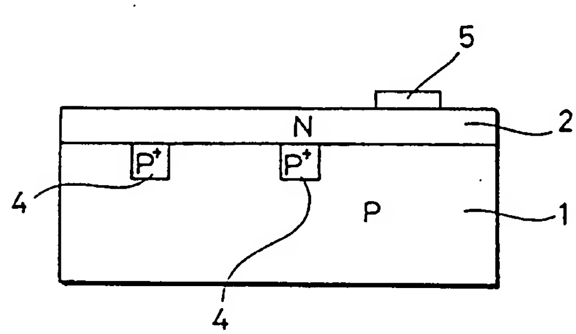


FIG. 2

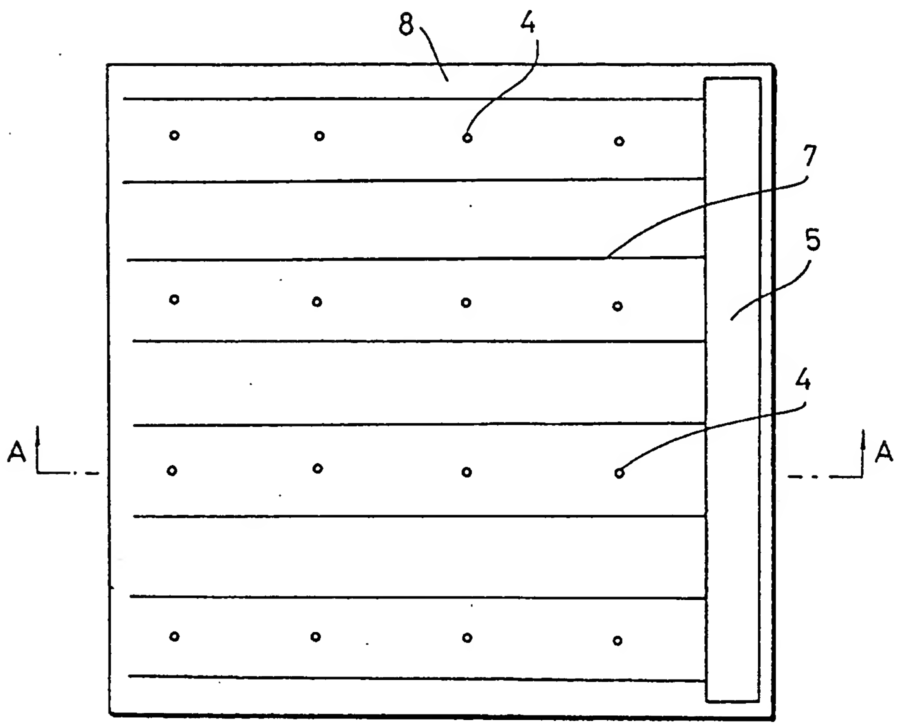


FIG. 3

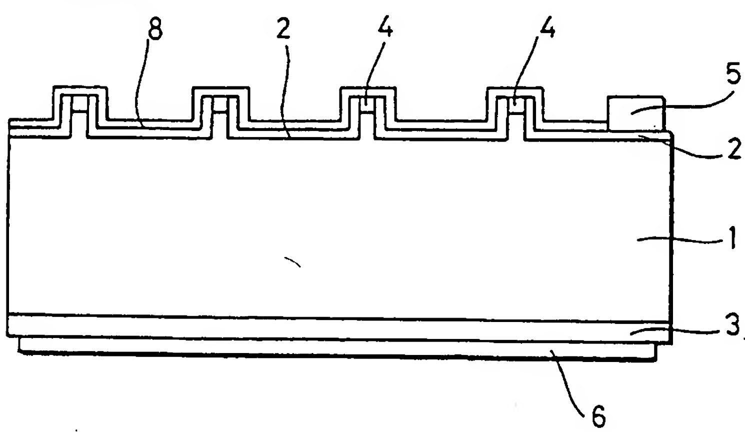


FIG. 4A

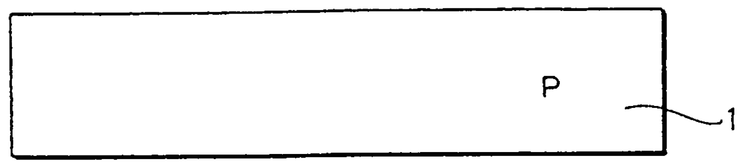


FIG. 4B

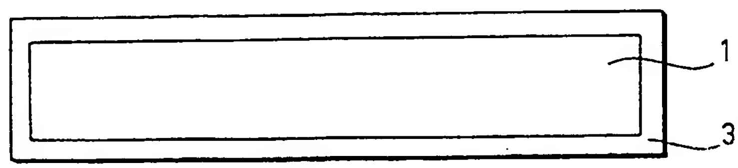


FIG. 4C

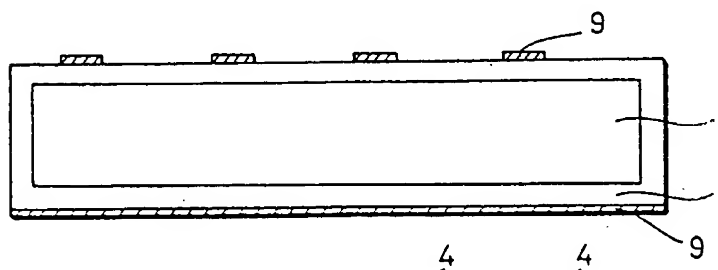


FIG. 4D

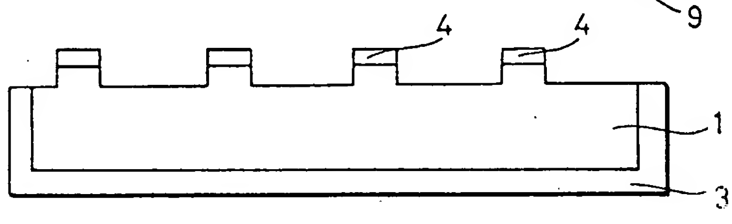


FIG. 4E

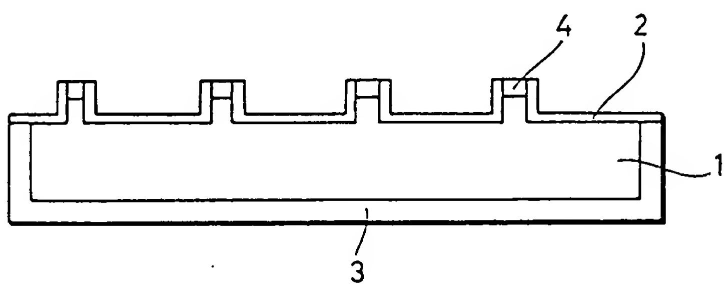


FIG. 4F

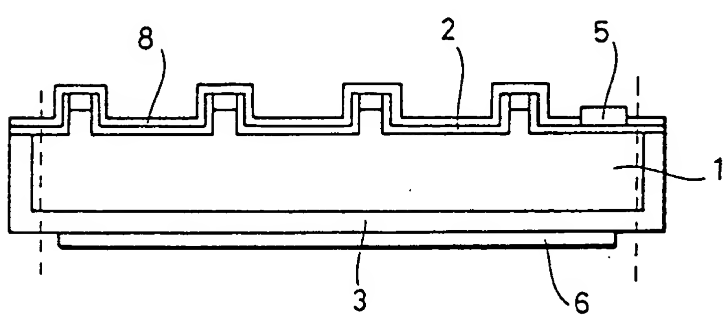


FIG. 5

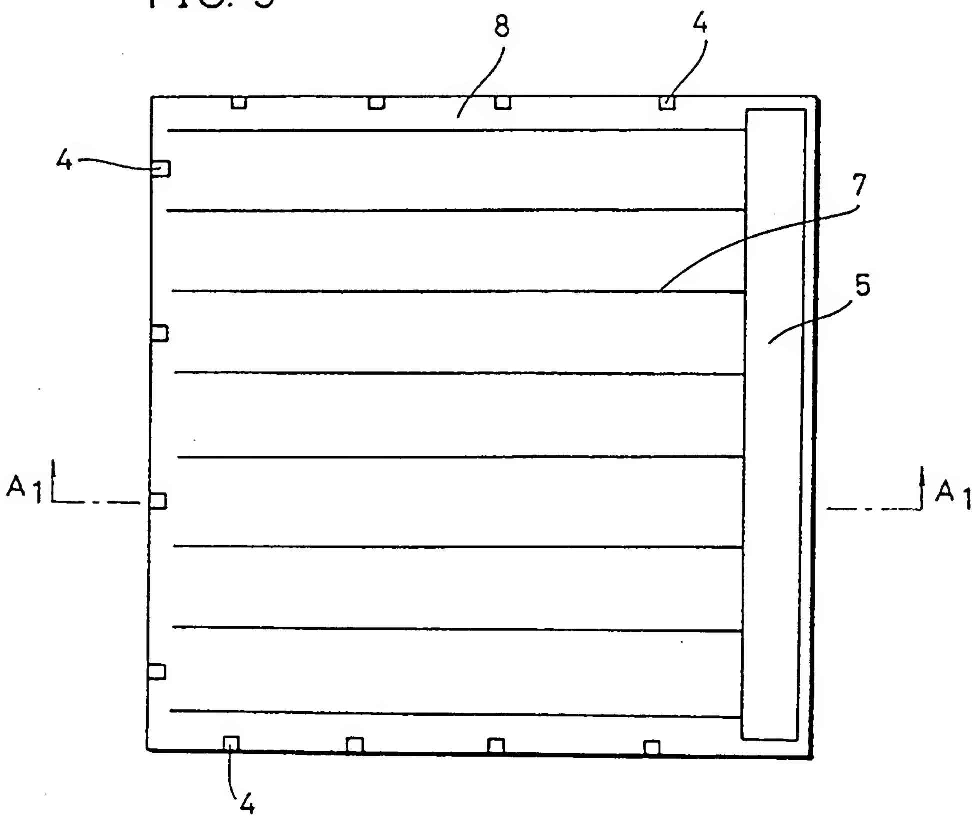


FIG. 6

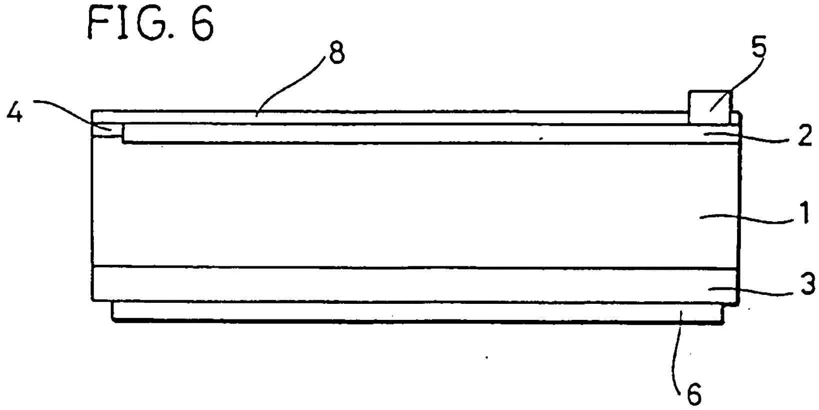


FIG 7A

FIG. 7B

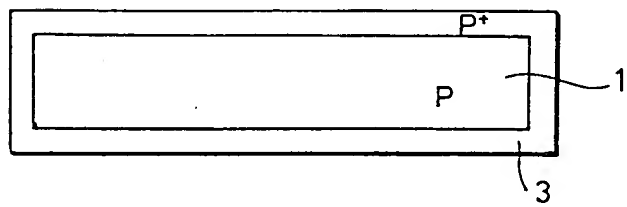


FIG. 7C

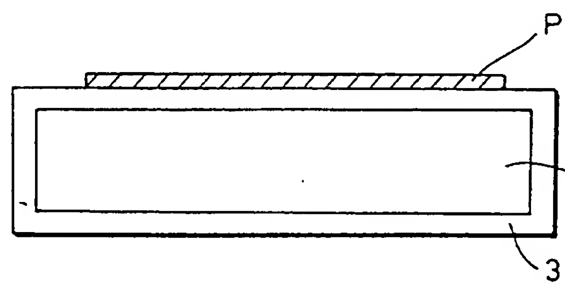


FIG. 7D

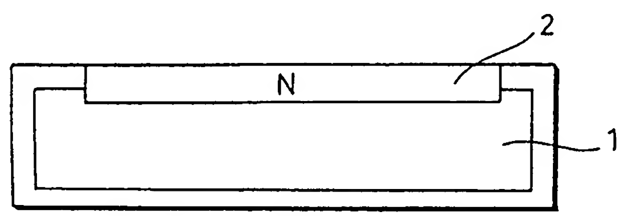


FIG. 7E

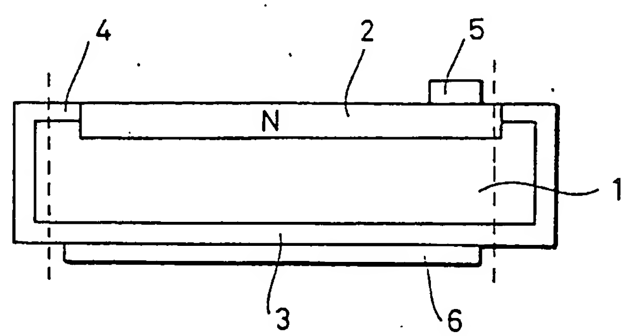


FIG.8

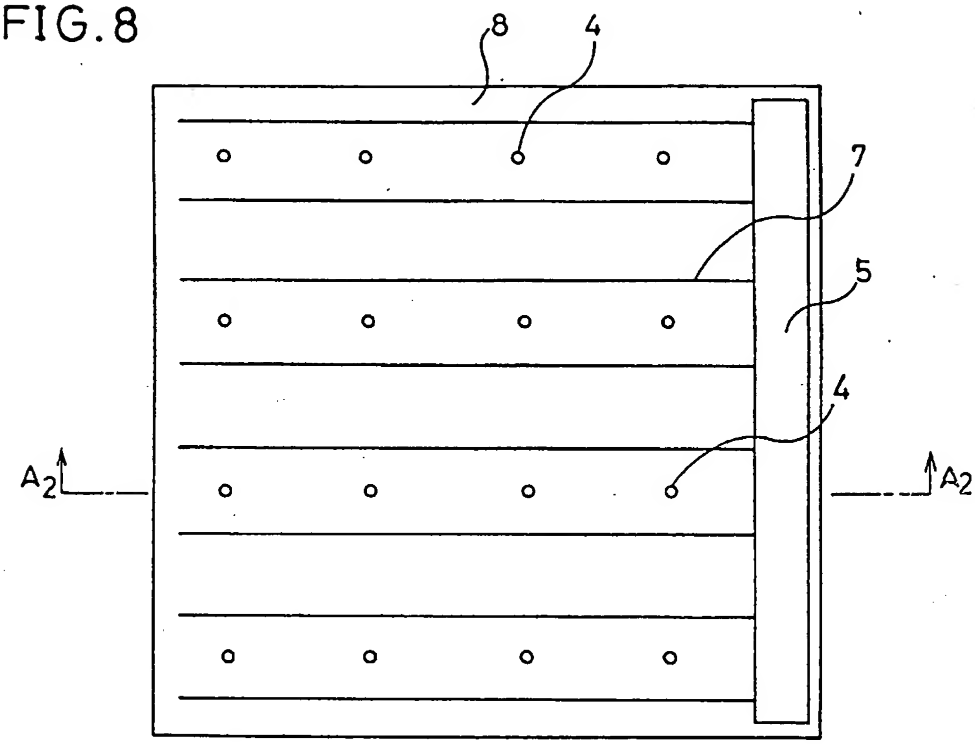


FIG.9

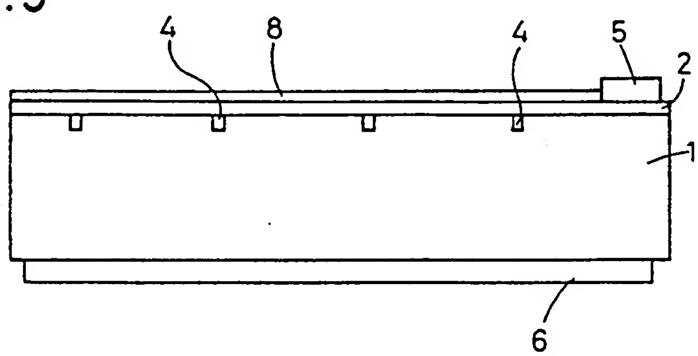


FIG.10A

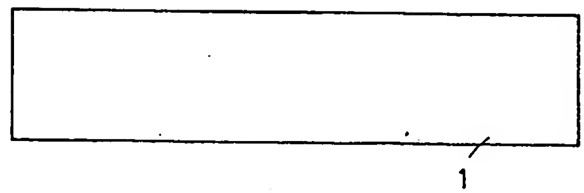


FIG.10B

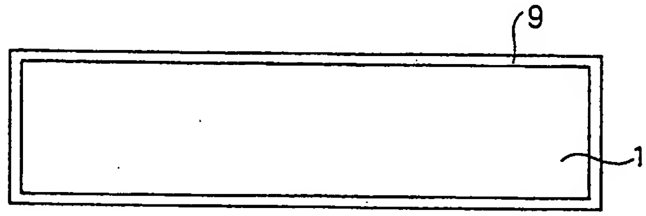


FIG.10C

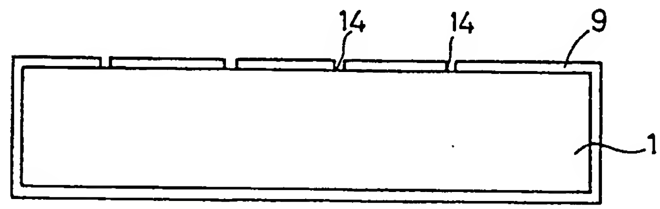


FIG.10D

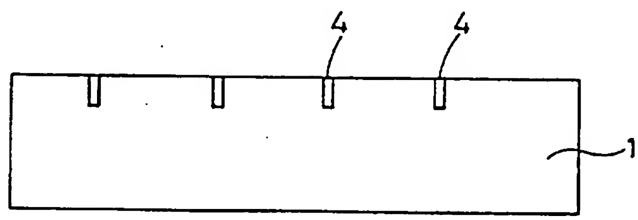


FIG.10E

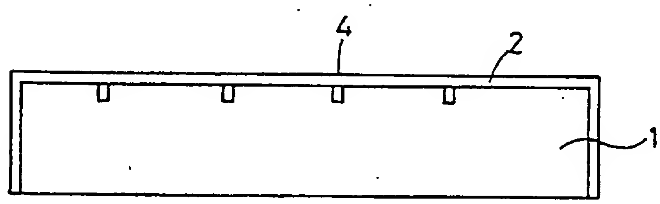


FIG.10F

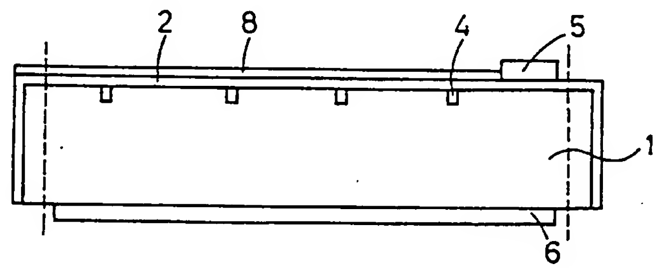


FIG. 11

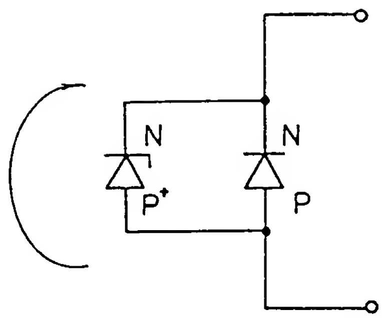


FIG. 12

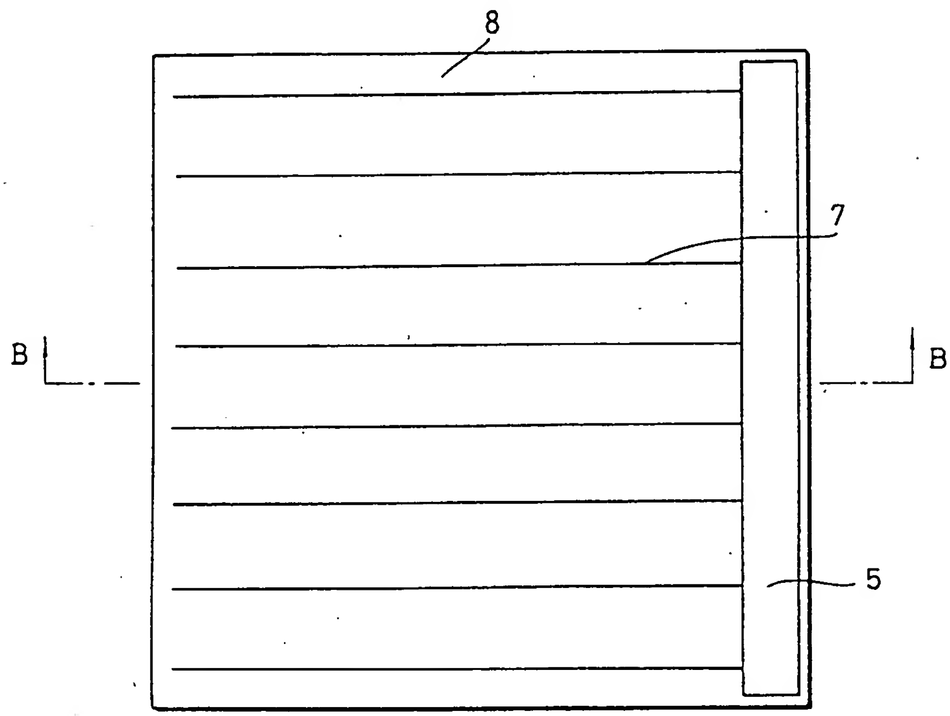


FIG. 13

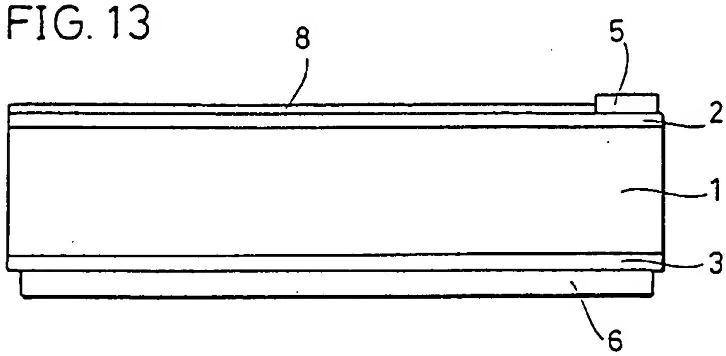


FIG. 14

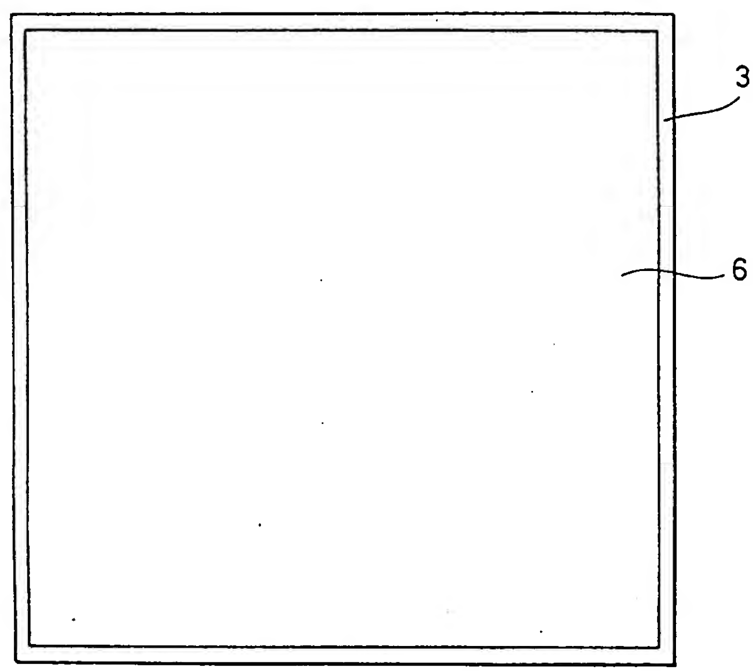


FIG. 15A

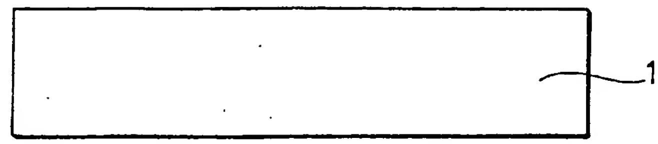


FIG. 15B

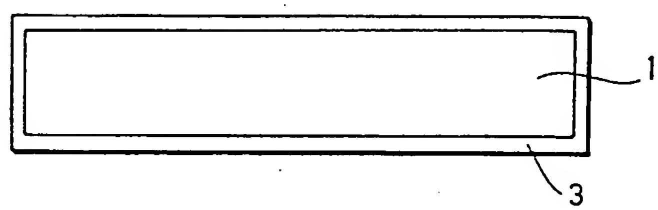


FIG. 15C

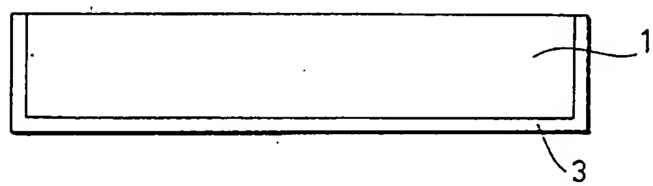


FIG. 15D

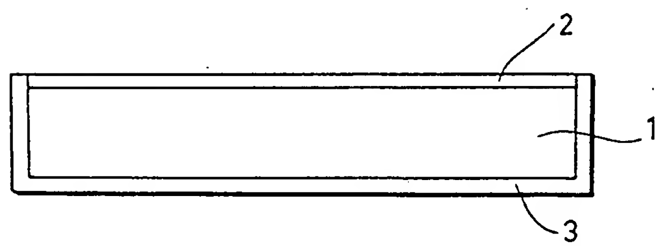
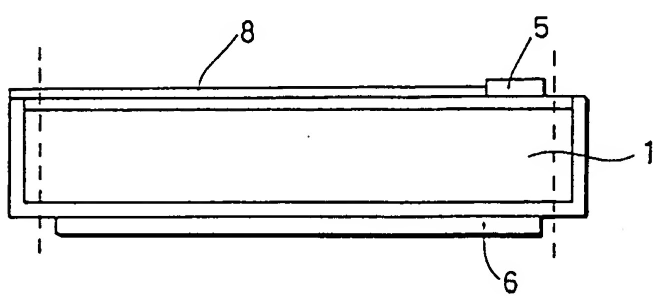


FIG. 15E



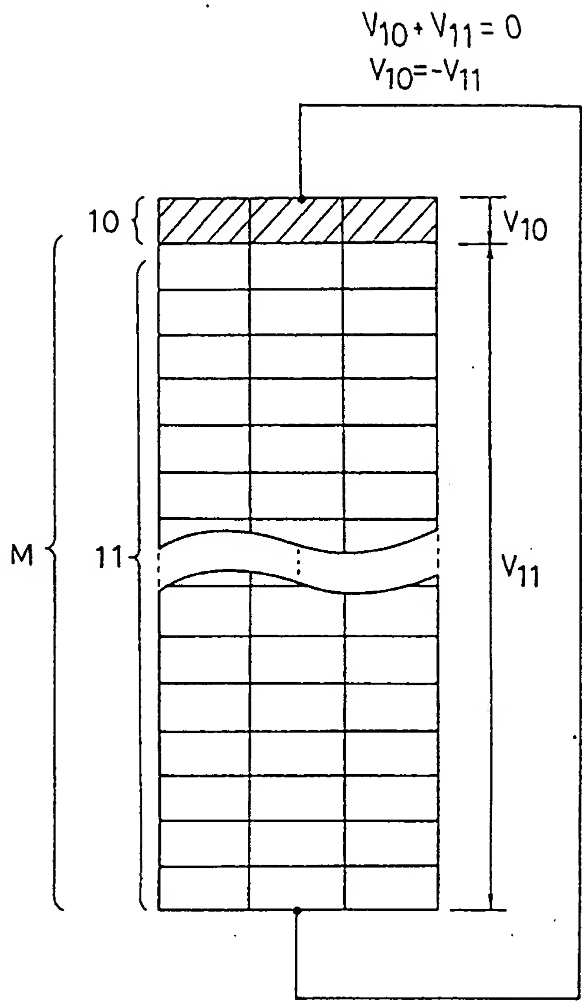


FIG.16A

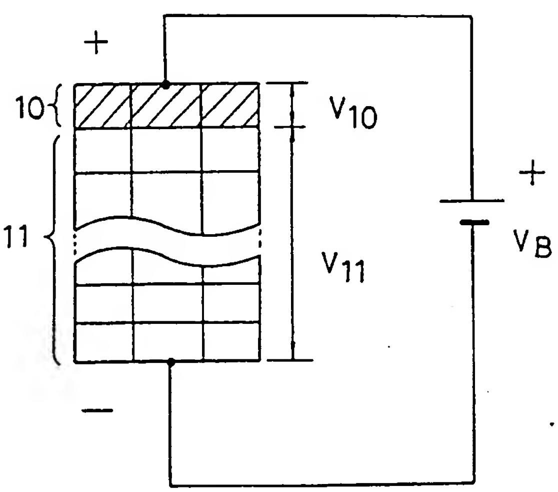


FIG.16B

$V_{10} + V_{11} = V_B$

$V_{10} = V_B - V_{11}$

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 11 7751

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 004 949 (I. A. LESK) * claims 6,7; figure 12 * ---	1-4,6,7	H01L31/068 H01L31/0352
X	US-A-4 112 457 (R.V. D'AIELLO) * column 2, line 4 - line 32; figures * ---	1,2,7	
X	PATENT ABSTRACTS OF JAPAN vol. 7, no. 204 (E-197)(1349) 9 September 1983 & JP-A-58 101 471 (NIPPON DENSHIN DENWA KOSHA) 16 June 1983 * abstract * ---	1	
A	FOURTEENTH IEEE PHOTOVOLTAIC SPECIALISTS CONFERENCE, San Diego, CA, 7th-10th January 1980, pages 141-145, IEEE, New York, US; K.-D. RASCH et al.: "Compatibility of BSR and BSF solar cell technology" * the whole document * ---	1,6	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	SOLAR CELLS vol. 19, no. 1, November 1986, LAUSANNE CH pages 97 - 108 M.A. GREEN ET AL. 'Thermal performance of integral bypass diode solar cell modules' * page 97, paragraph 1 - page 98 * -----	1	H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 JANUARY 1993	DE LAERE A.L.

CATEGORY OF CITED DOCUMENTS

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L : document cited for other reasons

& : member of the same patent family, corresponding document